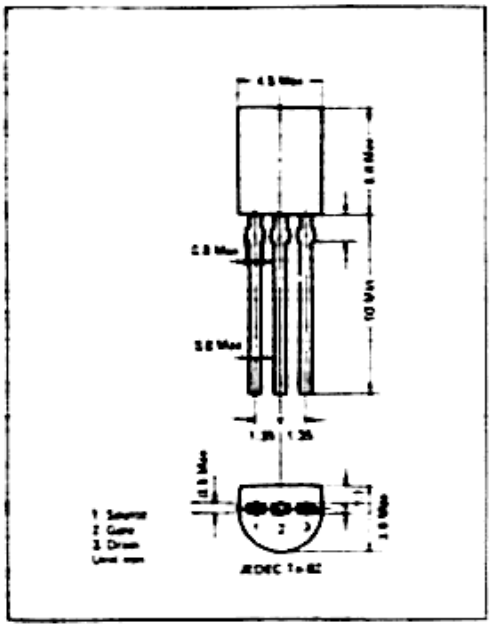
2SK125

Silicon N-Channel Junction FET

- UHF Amplifiers, Mixers (Common Gate)
- P_G: 12.5 dB Typ. (f = 100 MHz, Common Gate)
- NF: 1.5 dB Typ. (f = 100 MHz, Common Gate)
- 3rd Harmonic Distortion -52 dB Typ.
- Analogue Switchings (R_{ON}: 40Ω Typ.)



絶対最大定格 Absolute Maximum Ratings T_a = 25°C

Characteristics	Symbol	2SK125
Drain-to-Gate Voltage	V_{DGO}	25V
Source-to-Gate Voltage	V_{SGO}	25V
Drain Current	I_D	100 mA
Gate Current	I_G	10 mA
Channel Power Dissipation	P_{ch}	500 mW
Channel Temperature	T_{ch}	120°C
Storage Temperature	T_{stg}	-50–+120°C

電気的特性 Electrical Characteristics T_a = 25°C

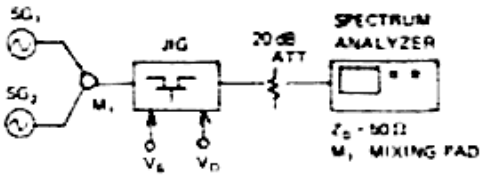
Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Unit
Gate Cutoff Current	I_{GSS}	V_{GS} = -15V, V_{DS} = 0			-10	nA
Gate-to-Source Voltage	V_{GSS}	I_G = -10μA, V_{DS} = 0	-25			V
Drain Saturation Current	I_{DSS}	V_{DS} = 10V, V_{GS} = 0, PW = 300μS	30		75	mA
Pinch-off Voltage	V_p	V_{DS} = 10V, I_D = 100μA	-2		-6	V
Forward Transfer Conductance	g_m	V_{DS} = 10V, I_D = 10 mA, f = 1 kHz	10	14		m℧
Reverse Transfer Capacitance	C_{rss}	V_{DG} = 10V, I_S = 0, f = 1 MHz		2.6	3	pF
Power Gain	P_G	V_{DG} = 10V, I_D = 10 mA, f = 100 MHz, BW = 2.8 MHz	10	12.5		dB
Noise Figure	NF	V_{DG} = 10V, I_D = 10 mA, f = 100 MHz, BW = 2.8 MHz 2nd Stage NF = 4.2 dB		1.8	2.5	dB
Intermodulation Distortion	IMD	V_{DG} = 10V, I_D = 10 mA, f_1 = 100MHz, f_2 = 100.1MHz, e_i = 100 dBμ	-45	-52		dB
Junction-to-Ambient Thermal Resistance	θ_{j-a}				190	°C/W

2SK125

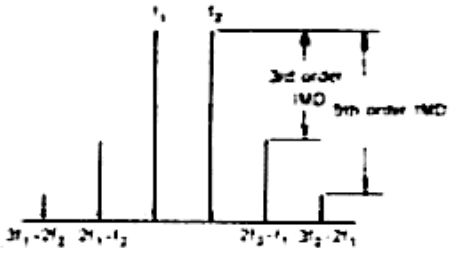
電路設計資料 Circuit Design Data $T_a = 25^\circ C$

Conditions	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Resistance	r_{ig}	$V_{DG} = 10V$, $I_D = 10mA$, f = 100 MHz		70		Ω
Input Capacitance	C_{ig}			3.0		pF
Output Resistance	r_{og}			5		kΩ
Output Capacitance	C_{og}			3.0		pF
Power Gain	P_G	$V_{DG} = 10V$, $I_D = 10mA$, f = 500 MHz, BW ≒ 12 MHz		7.0		dB
Noise Figure	NF			4.0		dB
Reverse Insertion Coefficient	$\|S_{12}\|$	$V_{DG} = 10V$, $I_D = 10mA$, f = 500 MHz		0.035		

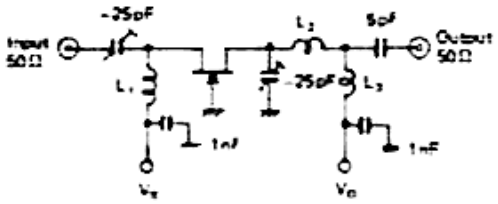
Block Diagram for IMD Measurement



Frequency Spectrum

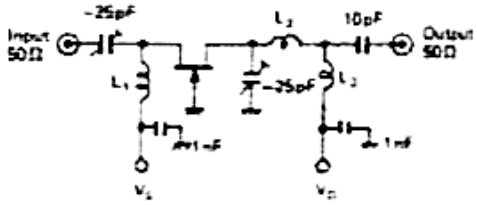


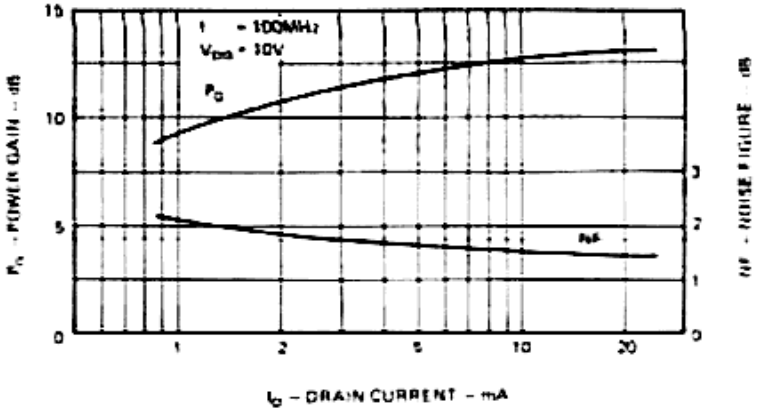
P_G & NF Test Circuit (f = 100 MHz)



L1 : 0.45φ 3φ 10.5T
L2, L3 : 0.45φ 3φ 5.5T

IMD Test Circuit (f = 100 MHz)



L1 : 0.45φ 3φ 10.5T
L2, L3 : 0.45φ 3φ 5.5T

P_G, NF – I_D